FILLING OF INSULATION TRENCHES USING CMOS STANDARD PROCESSES FOR CREATING DIELECTRICALLY INSULATED AREAS ON AN SOI WAFER

The invention relates to a method of manufacturing filled isolation trenches in silicon by applying CMOS standard processes for forming dielectrically insulated regions (insulation trenches; isolation trenches) on an SOI wafer. To this end, only silicon dioxide is to be used for the filling. The technique results in sealed cavities of voids within the trench. These remaining voids are advantageous with respect to a reduction of elastic stress. The technique leads to the filling of trenches having an aspect ratio ranging from small values to very high values with various angles of the sidewalls.

The conventional isolation trenches for the dielectric insulation of different circuit portions usually do not meet the requirements of micro electronic mechanic systems (MEMS) with respect to minimizing stress and using an equivalent fill material, which may, if required, be removed at defined positions in a later stage in a highly selective manner relative to silicon.

Most of the well-known techniques are based on the concept of avoiding voids. This is accomplished by either avoiding narrow portions or bottlenecks during the trench fill process (V-shaped trench profiles, specific deposition techniques) or by removing existing bottlenecks by a dedicated back etch process.

Avoiding voids may, for instance, be achieved by a V-shaped trench geometry including a specific edge design, cf. US-A 6 180 490. Also in this case the aspect ratio of the trench to be filled is restricted.

In the known techniques for forming trench isolations of semiconductor devices in a semiconductor layer of an SOI wafer shallow trenches are used, which in most cases should be devoid of voids. US-A 6 261 921 describes such a technique usable for shallow trenches, wherein a V-shaped trench is used and a silicon nitride layer is used for an additional edge retraction.

US-A 2002/0076915 describes a fill process with polysilicon deposited on an insulating layer. The method is used for SOI wafers for manufacturing integrated circuits, the method does, however, not allow high aspect ratios of the trench to be filled. As a special feature a tapering of the trench opening by back etching of overhanging material

at the trench opening that builds up during the fill process is described in order to avoid voids.

A similar technique, however for trenches within the semiconductor (not an SOI wafer) with respect to shallow trenches having a depth of 1 µm or less is described in US-A 6 140 207. Also in this case a tapering of the trench opening is realized by an oblique portion in the silicon.

US-A 5 872 058 discloses a special deposition technique for a dielectric insulation layer (SiO_2 or any other material). This technique uses special deposition conditions, wherein the deposition rate and the etch rate are adjusted with different gas concentrations such that any bottlenecks in trench are avoided during the fill process, thereby enabling a substantially void-free filling of trenches. The aspect ratio is stated to be 3:1 or higher. Also in this case a filling of A-shaped trench structures does not appear to be possible.

It is an object of the present invention to provide a cost effective realization of dielectrically insulated trenches (insulation trenches) in the context of the CMOS technique for as wide a spectrum of trench geometries as possible (various aspect ratios and different angles of the trench walls in the form of V-shaped and A-shaped configurations), wherein the trenches are to be sealed with respect to the wafer surface.

The invention is based on the object to provide a method that exclusively uses process steps of the CMOS standard technology for coating (filling) insulation trenches in a silicon wafer. The unavoidable occurring voids within the insulation trench are advantageous, since the voids may avoid stress.

The object is solved by the features as recited in claims 1 or 13 or 15. Also the product is claimed, independent of the manufacturing method, however also defined therethrough. The method is designed such that the closing point of the voids with respect to the wafer surface is positioned so deeply below the wafer surface that an opening of the voids in subsequent process steps may reliably be avoided.

The invention will be described and completed by embodiments including two semiconductor wafers by referring to the drawings.

Figure 1a,
Figure 1b represent an illustration of a trench 2 to be filled after a non-illustrated trench etch process into silicon 1 and after the removal of a resist or an

oxide etch mask for the trench etch process of two different surfaces of semiconductor wafers A1, A2.

Figure 2a,
Figure 2b are illustrations of the partially filled trench 2, 9 after the first fill process using silicon dioxide. In all of the drawings a middle level 100 of the trenches 2 is shown.

Figure 3a,
Figure 3b are representations of the partially filled trench after the anisotropic etching of the silicon dioxide.

Figure 4a,
Figure 4b show the result after a second trench fill process with a hermitically tight seal 14.

Figures 1a and 1b illustrate the trench 2 etched into the silicon 1 as an example of an (active) semiconductor layer after the removal of a resist etch mask or an oxide etch mask. That is, a silicon surface 3 or a poly silicon surface 4 are free of oxide. In figure 1b at least one oxide layer 5 is located under the layer 6 made of polysilicon, which is important during later process steps after the trench filling.

In figures 1 the devices and the portions of the two illustrated silicon wafers A1, A2 are shortly described. The silicon 1 is an active semiconductor layer, which in SOI wafers is positioned above a buried horizontal oxide and a carrier layer located below the buried oxide. The described trench 2 is formed in this active layer, wherein a length direction of the trench extends along the direction perpendicular to the drawing plane; the trench is to represent a variety of such trenches used for a dielectric insulation. These isolation trenches are also referred to as insulation trenches and serve for the "electrical isolation" of regions, which means that current may not flow through these insulating trenches in an amount that may interfere, preferably a current flow does not occur at all. These trenches form a dielectric barrier between different potentials and thus allow a potential generation of a voltage between the sidewall at the left-hand side of the trench 2, indicated as 1a', and the right-hand wall 1a". The trench depth is not explicitly illustrated. The trenches may be deep at aspect ratios of 15:1 and more. Only a portion is shown, to which relate the examples described herein in the area of the upper trench edge and an upper portion of these trenches, which is to referred to in this specification as an upper trench portion. Also not specifically shown are devices or structures that are generally denoted as B and are located in the active semiconductor layer 1 or which are formed therein in a later stage.

Such a silicon layer is to be understood to include all types of active semiconductor layers, irrespective of the specific material they are made of. These layers are to represent semiconductor layers, in this case a silicon in an SOI wafer, which acts as "silicon on insulator" as a generic term for the active semiconductor layer.

Upper trench edges of the trench 2 are shown in figure 2a. There, the left trench wall terminates at its upper edge 2a' and the right trench wall at the upper right trench edge 2a".

In figures 2a and 2b there is schematically shown a silicon dioxide layer 7, which has been deposited on the surface and on the sidewalls 1a', 1a"; here sections 7', 7" are formed. In this case a narrow portion or bottleneck 8 above the silicon surface 3 is illustrated, which is inappropriately positioned for a further filling. The partially filled trench 9 (remaining trench) is not yet sealed and the still unfilled volume therein tapers downwardly.

Figures 3a and 3b schematically illustrate the result of an anisotropic etch process of the silicon dioxide 7, when performed with high selectivity with respect to the silicon 1. The anisotropic etch process preferably removes the silicon dioxide 7 in a direction perpendicular to the surface. Undercut portions 9a are etched with the lowest etch rate. Therefore the residues 7a of the filling will remain at the sidewalls 1a', 1a" as sketched and thus form a narrow portion or bottleneck 8a located below the silicon surface 3a and the polysilicon surface 4a, respectively. The bottleneck is offset in the downward direction with respect to the previous bottleneck 8. The respective measures a7, a8 demonstrate this effect in both methods.

In this way a step is created originating from the upper end of the remaining layers 7a and reaching to the surfaces 3a or 4a. This may be comparable to an "oxide recessing within the trench".

SiO_2 is again deposited, preferably by an low pressure technique and a sealing layer 10 is formed within and on the at least one trench 2. The layer 10 extends across the remaining layers 7a, the steps at both sides and onto the horizontal surfaces outside the trench.

Figures 4a and 4b schematically show the result after completing the trench fill process on the basis of silicon dioxide 10. The sealing or closing point 12 is located (significantly) deeper compared to the silicon surface 3b and the polysilicon surface 4b,

respectively. On the other hand the notch tip 13 in the filled area is located significantly higher compared to the silicon surface 3b and the polysilicon surface 4b, respectively, which may be of importance for a subsequent planarization. This illustrated in a symbolic manner by the distance "c". A planarization process may no longer reopen the sealed void 11. The distance c prevents such an unwanted opening, while also the recessing is helpful in this respect.

The remaining void or cavity 11 is hermetically sealed to the surface and does not contain any gas, since a low pressure process was used for the silicon dioxide deposition, in particular in the form of a low pressure CVD. The sealing portion 14 does not exhibit any further voids, since the trench geometry (trench width, recess depth of the sealing point 12) was selected in a defined manner.

The filling in the first fill step is adapted to or controlled with respect to "the trench geometry". The silicon dioxide deposition 7 providing the horizontal sections at both sides of the trench and the vertical sections 7', 7" inside the trench is adapted to the trench geometry, which has the upper corner areas and substantially vertical wall in the depth direction of the trench as well as a substantially horizontal surface of the active semiconductor layer 1. Due to the trench geometry the thickened portion of the deposited inner layer (inside the trench) is formed during the first deposition, wherein the left layer and the right layer in the vicinity of the trench edges 2a', 2a" (in the height area) grow more strongly or intensively, thereby increasingly forming a bottleneck 8, which has as a bottleneck a reduced width compared to the free volume 9 in the form of "remaining trench or residual trench", the width of which increases with increasing depth.

Since the bottleneck is substantially independent of the trench depth, that is, the aspect ratio, and is substantially independent of the angle of the trench walls near the silicon surface, the position of a sealing point to be formed in a later stage is realized independently of the trench geometry. The controlled silicon dioxide deposition adapted to the trench geometry is meant as a deposition that is adapted to the illustrates trench geometry; the bottleneck 8 is automatically obtained, even and in particular with substantially vertical trench walls 1a', 1a". In this case the effect is taken advantage of that the silicon dioxide is deposited faster (at interfaces of faces parallel to the surface and faces having a vertical part, in the present case, the entire side faces facing inwardly or the inner surfaces of the trenches). The tapering of the entrance of the remaining void 9, that is, the largest bottleneck 8 of the trench, is obtained near the edges and is not avoided but instead is advantageously exploited.

The SOI wafer may be structured such that in its semiconductor layer located above the oxide layer also micro mechanic systems (MEMS) are provided, which are not explicitly shown.

The second step of removing the SiO_2 layer, explained with reference to figures 3, shall be emphasized once again in order to explain the sealing or closing point 12, which is located in the respective embodiments below the respective surfaces 3b, 4b according to the respective figures 4.

The exemplary anisotropic RIE etch process of the oxide layer 7 in figures 2 results in two symbolical sub steps, thereby firstly removing the horizontal layer portions, as is shown in figures 3. This is the "first sub step" until the removal of the silicon dioxide layer on the wafer surface.

From then on the symbolic "second sub step" follows. Hereby, a portion of the silicon dioxide layer 7a provided at the vertical trench walls 1a', 1a'' is also removed and the bottleneck 8 is displaced downwardly. In the upper trench portion the oxide layer is thus removed down to a defined depth, as is shown as a7 in figure 3a and a8 in figure 3b. Due to this material removal and the displacement of the bottleneck in the depth direction the later sealing point is determined, which is then actually formed by the further deposition of silicon dioxide of figures 4. The sealing point is located at the downwardly displaced bottleneck 8a, from which is obtained the upper sealing point 12, that is, the upper end of the sealed void 11, after the further deposition. This is simultaneously the lower end of the portion 14 of the hermetic sealing.

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list of reference signs

(the same reference signs refer to the same components throughout the figures)

1:	silicon
2:	trench etched into silicon
3:	silicon surface after removal of the etch mask
3a:	silicon surface after removal of the first fill oxide
3b:	silicon surface covered by the second fill oxide
4:	silicon surface after removal of the etch mask
4a:	silicon surface after removal of the first fill oxide
4b:	silicon surface covered by the second fill oxide
5	oxide layer
6	polysilicon layer
7	oxide layer after the first filling of the trench
7a:	oxide layer after back etching the first fill oxide
8	narrowest portion, located higher relative to the level of the silicon surface
8a:	narrowest portion after back etching the first fill oxide
9	partially filled trench during the technological process
10:	oxide layer after the second filling of the trench
11:	remaining void
12:	sealing point located more deeply relative to the level of the silicon surface
13:	tip of the notch of the second oxide filling
14:	position of the hermitic seal

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